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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/038,305 | 01/02/2002 | Jigish D. Trivedi | MICRON.133DV1 | 7715 |

20995 7590 04/19/2004

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| EXAMINER | |
|---|---|
| NGUYEN, THANH T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2813 | |

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/038,305 | TRIVEDI ET AL. | |
| | Examiner | Art Unit | |
| | Thanh T. Nguyen | 2813 | |

*-- The MAILING DATE of this communication appears on th cover sheet with the correspond nce address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-10 and 17-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-10, 17-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Applicant's arguments filed 1/9/04 have been fully considered but they are not persuasive.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-9, and 17-20 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (U.S. Patent No. 6,156,651) in view of Liu (U.S. Patent No. 6,211,085).

Referring to figures 6A-6F, Havemann teaches a method of forming an integrated circuit comprising the steps of: forming a dual damascene structure (figure 6b) in insulating material (30, 40) over the semiconductor substrate (10) the dual damascene structure comprising a trench (upper portion of contact hole) and a contact via (lower portion of contact hole) extending from a bottom of the trench to expose a conductive element 10 (see col. 3, lines 43-45), depositing a first metal (tungsten, 66, see col. 3, lines 19-21) (as claimed in claims 2, 15 and 19) selectively over the conductive element relative to insulating surfaces of the dual damascene structure to

partially fill the contact via (see figure 6C), and filling a remainder of the contact via with a second metal (70, aluminum, see figure 6E, as claimed in claims 2, and 20) by PVD (see col. 6, lines 44-46), the second metal of aluminum being more conductive than the first metal of tungsten and reflowing the conductor aluminum metal layer (70) at the temperature of 300-600°C (see col. 2, lines 19-24, as claimed in claim 5), wherein depositing the first metal comprises filling the contact via to a height between about one-third and two thirds of height of the contact via (see figure 6C, col. 5, lines 39-41, 54-61). It is noted that the selective deposition fills the via to less than the height of the interlevel dielectric, and stop filling prior to reaching the top of the interlevel dielectric layer (see figure 6C, col. 5, lines 39-41, 54-61) would obviously means that filling the contact via with the metal to the height between about one-third and two thirds (meeting claims 6-7, and 17-18).

Regarding to claims 8-9, filling comprises overflowing the contact via to at least partially fill the trench with the second metal (70, aluminum), with a hot aluminum deposition by depositing the metal layer at a temperature of 300-600°C (see col. 2, lines 19-24).

Havemann teaches selectively forming first metal initiated by a conductive area in the substrate at the bottom of the via (see col. 6, lines 40-44). However, Havemann does not teach a method of depositing a first metal layer by selective chemical vapor deposition with the depositing ratio of the first metal thickness over the conductive element to first metal thickness over insulating surface of dual damascene structure of greater than about 10:1 (as claimed in claims 3-4). Nevertheless, depositing a metal by selective chemical vapor deposition with the depositing ratio of the first metal thickness over the conductive element to first metal thickness over insulating surface of dual damascene structure of greater than about 10:1, and preferentially

depositing comprises selectively nucleating the first metal on exposed conductive surfaces in the contact via during a chemical vapor deposition is known in the semiconductor processing art as evidenced by Liu. Liu teaches depositing a metal (tungsten, 80) by selective chemical vapor deposition (see col. 4, lines 50-52, figure 4, as claimed in claim 3) with the depositing ratio of the first metal thickness over the conductive element to first metal thickness over insulating surface of the dual damascene structure of greater than about 10:1 (see figure 4), and preferentially depositing comprises selectively nucleating the first metal on exposed conductive surfaces in the contact via during a chemical vapor deposition (see col. 4, lines 25-31, as claimed in claim 16). Since, Liu teaches that tungsten is not formed on the insulating layer and first metal (tungsten) is not seen on the insulating surface of the dual damascene structure (see figure 4), hence it is obvious to a person of ordinary skill in the art that Liu's selectively depositing a metal tungsten on the via hole with partially filled having the thickness of the metal over the conductive element is at least ten times greater than the thickness of the metal over the insulating surface (as claimed in claim 4). It would have been obvious to a person of ordinary skill in the art at the time the invention was made would deposit a metal by selective chemical vapor deposition with the depositing ratio of the first metal thickness over the conductive element to first metal thickness over insulating surface of the dual damascene structure of greater than about 10:1, and preferentially depositing comprises selectively nucleating the first metal on exposed conductive surfaces in the contact via during a chemical vapor deposition in Havemann's process as taught by Liu ***because*** depositing a metal by selective chemical vapor deposition and selectively nucleating the first metal on exposed conductive surfaces in the contact via during a chemical vapor deposition would form a first metal only inside the contact via without (or only a minimal

amount of) first metal formed on the insulating layer outside the contact via, therefore, using an extra step to remove the first metal formed on the insulating layer outside the contact via is not needed.

Claims 21-23 are stand rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (U.S. Patent No. 6,156,651) in view of Omura (U.S. Patent No. 6,028,362).

Havemann teaches forming a third metal 62 over second metal 60 in figure 5G. However, Havemann does not teach depositing a third metal with physical vapor deposition over the second metal layer formed with physical vapor deposition. Nevertheless, depositing a third metal with physical vapor deposition over the second metal layer formed with physical vapor deposition is known in the semiconductor processing art as evidenced by Omura. Omura teaches depositing a second metal (aluminum, 56, as claimed in claim 9) by physical vapor deposition (see figure 22 and col. 17, lines 60-62) to fill the remaining portion of the contact via over the first metal and at least partially fill the trenches and heating to a temperature of 400-550°C to reflow the second metal layer (aluminum, 56, see figure 22, col. 17, lines 23-63, as claimed in claims 5 and 9), depositing a third metal layer (aluminum, 71, 72) over the second metal layer by PVD process (see col. 18, lines 10-15, figure 23B, as claimed in claims 10). It would have been obvious to a person of ordinary skill in the art at the time the invention was made would deposit a third metal with physical vapor deposition over the second metal layer which is formed with physical vapor deposition in Havemann's process as taught by Omura ***because*** third metal layer would have filled any depression formed on top of second metal layer, and third metal layer also can be used as multi-level wiring interconnection.

In regarding to claims 21 to 23, Havemann does not teach forming a barrier and adhesion layer in the contact hole. Nevertheless, forming a barrier and adhesion layer in the contact hole is known in the semiconductor processing art as evidenced by Omura. Omura teaches in figures 23A, the contact via and the trench are lined with an adhesion layer and a barrier layer (50, Ti and TiN, see col. 9, lines 1-5) before depositing first metal (52, as claimed in claims 21-23). It would have been obvious to a person of ordinary skill in the art at the time the invention was made would have lined contact via and trench with an adhesion layer Ti and a barrier layer TiN before depositing the first metal ***because*** titanium (Ti) layer has very good metal adhesion property which enable the overlying material to adhere to underlying material such as silicon substrate or metal layer or even the insulating layer, and titanium nitride layer (TiN) barrier prevents the metal diffusion between metals or between metal and silicon material.

Claim 10 is stand rejected under 35 U.S.C. 103(a) as being unpatentable over Havemann (U.S. Patent No. 6,156,651) in view of Yu et al. (U.S. Patent No. 6,365,514).

Havemann does not teach a method of depositing an aluminum second metal layer with a hot aluminum deposition into the contact trench and via, then depositing a cold aluminum layer over the hot aluminum layer. Nevertheless, depositing a second metal layer with a hot aluminum deposition then depositing a cold aluminum layer over the hot aluminum layer is known in the semiconductor processing art as evidenced by Yu et al. Yu et al. teaches a method of depositing an aluminum layer with a first step of depositing a hot aluminum layer into the contact trench and via then follow with a second step of depositing a cold aluminum layer over the hot aluminum layer (see col. 3, lines 10-14, col.5, lines 19-28 and col. 7, lines 1-23). It would have

been obvious to a person of ordinary skill in the requisite art at the time the invention was made would deposit a hot aluminum layer into the contact trench and via then follow with a cold aluminum layer over the hot aluminum layer in Havemann's process as taught by Yu et al. ***because*** depositing a hot aluminum layer in the contact trench and via will increase the mobility of aluminum atoms during the hot deposition process, therefore, the formation of voids within the aluminum layer can be avoided, and hot deposition process also promote the reaction between underlying tungsten metal layer and hot aluminum, and between tungsten with the underlying conductive layer to form a good contact between conductors. The second step of depositing a cold aluminum layer over hot aluminum layer prevents the long duration of hot aluminum deposition in a single step deposition process of aluminum, long duration of hot aluminum deposition at high temperature degrades the device performance due to out-diffusion of dopants in the implanted area of integrated circuit.

### *Response to Arguments*

Applicant's arguments filed 1/9/04 have been fully considered but they are not persuasive.

Applicant contends that Havemann does not teach depositing the first metal comprises filling the contact via to a height between about one-third and two thirds of height of the contact via. In response to applicant that Havemann teaches depositing the first metal comprises filling the contact via to a height between about one-third and two thirds of height of the contact via (see figure 6C, col. 5, lines 39-41, 54-61). It is noted that the selective deposition fills the via to

less than the height of the interlevel dielectric, and stop filling prior to reaching the top of the interlevel dielectric layer (see figure 6C, col. 5, lines 39-41, 54-61) would obviously means that filling the contact via with the metal to the height between about one-third and two thirds (meeting claims 6-7, and 17-18). The specification contains no disclosure of either the critical nature of the claimed arrangement (i.e.- filling the contact via to a height between about one-third and two thirds of height of the contact via) or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen limitations or upon another variable recited in a claim, the applicant must show that the chosen limitations are critical. In re Woodruff, 919 F.2d 1575, 1578 (FED. Cir. 1990). It is also obvious/inherent that forming the more conductive layer to provide more conductivity. Therefore, the claims are still stand rejected under Havemann.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800